Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 35, 36, 45, 46, 51, 53, 57 and 59 as follows:

Listing of Claims:

Claims 1-27 (Canceled)

28. (Previously Presented) An integrated circuit dynamic random access memory ("DRAM") device having an integrated cache system, comprising:

at least one DRAM array divided into a plurality of blocks;

an auxiliary memory of the type not required to be refreshed;

an address decoder coupled to receive a memory address and being operable to decode the address and generate decoded address signals corresponding thereto;

an input/output circuit coupled to the at least one DRAM array, the auxiliary memory, and the address decoder, the input/output circuit being operable to respond to a first control signal by coupling write data from an external data terminal to a location in a block of the at least one DRAM array corresponding to the decoded address signals, or to respond to a second control signal by coupling write data from the external data terminal to a location in the auxiliary memory, or to respond to a third control signal by coupling data from the auxiliary memory to a location in a block of the at least one DRAM array corresponding to the decoded address signals; and

a control circuit coupled to the at least one DRAM array, the auxiliary memory, the address decoder, and the input/output circuit, the control circuit being operable to refresh the at least one DRAM array one block at a time, the control circuit further being operable to generate the first control signal when the block of the at least one DRAM array corresponding to the decoded address signals is not being refreshed, to generate the second control signal when the block of the at least one DRAM array corresponding to the decoded address signals is being refreshed, to generate the third control signal when the block of the at least one DRAM array that was being refreshed when the data was stored in one of the auxiliary memory is no longer being refreshed.

29. (Previously Presented) The DRAM device of claim 28 wherein the auxiliary memory comprises a static random access memory ("SRAM") device.

30. (Previously Presented) The DRAM device of claim 28 wherein the control circuit comprises:

a refresh controller coupled to the at least one DRAM array, the refresh controller being operable to refresh the at least one DRAM array one block at a time; and

a control buffer structured to receive a memory command and to generate the first, second and third control signals corresponding thereto.

31. (Previously Presented) The DRAM device of claim 28 wherein the plurality of blocks of the at least one DRAM array are physically part of a single DRAM array.

32. (Previously Presented) The DRAM device of claim 28 wherein the input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the at least one DRAM array while a second pair of input/output lines may be coupled to another block of the at least one DRAM array.

33. (Previously Presented) The DRAM device of claim 28, further comprising a second auxiliary memory operable to store data in the event the first auxiliary memory is busy storing data or reading or writing data.

34. (Previously Presented) An integrated circuit dynamic random access memory ("DRAM") device having an integrated cache system, comprising:

at least one DRAM array divided into a plurality of blocks;

an auxiliary memory coupled to the at least one DRAM array for direct transfer of data from the auxiliary memory to any block of the at least one DRAM array if the block of the at least one DRAM array is not being refreshed; and

an input/output circuit coupled to the at least one DRAM array and the auxiliary memory, the input/output circuit being operable to store write data in a block of the at least one DRAM array to which the write data was directed, and to store write data directed to any block

of the at least one DRAM array in the auxiliary memory if the block to which the write data was directed is being refreshed.

35. (Currently Amended) The DRAM of claim 34 wherein the plurality of blocks of the at least one DRAM array ~~is~~are physically part of a single DRAM array.

36. (Currently Amended) The DRAM of claim 34 wherein the ~~an~~ input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the at least one DRAM array while a second pair of input/output lines may be coupled to another block of the at least one DRAM array.

37. (Previously Presented) The DRAM of claim 34 wherein the auxiliary memory comprises a static random access memory device.

38. (Previously Presented) A processor-based system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a system controller coupled to the processor bus;

an integrated circuit system memory and cache system coupled to the processor through the system controller, comprising:

at least one DRAM array divided into a plurality of blocks;

an auxiliary memory of the type not required to be refreshed;

an address decoder coupled to receive a memory address and being operable to decode the address and generate decoded address signals corresponding thereto;

an input/output circuit coupled to the at least one DRAM array, the auxiliary memory, and the address decoder, the input/output circuit being operable to respond to a first control signal by coupling write data from an external data terminal to a

location in a block of the at least one DRAM array corresponding to the decoded address signals, or to respond to a second control signal by coupling write data from the external data terminal to a location in the auxiliary memory, or to respond to a third control signal by coupling data from the auxiliary memory to a location in a block of the at least one DRAM array corresponding to the decoded address signals; and

a control circuit coupled to the at least one DRAM array, the auxiliary memory, the address decoder, and the input/output circuit, the control circuit being operable to refresh the at least one DRAM array one block at a time, the control circuit further being operable to generate the first control signal when the block of the at least one DRAM array corresponding to the decoded address signals is not being refreshed, to generate the second control signal when the block of the at least one DRAM array corresponding to the decoded address signals is being refreshed, to generate the third control signal when the block of the at least one DRAM array that was being refreshed when the data was stored in one of the auxiliary memory is no longer being refreshed.

39. (Previously Presented) The processor-based system of claim 38 wherein the auxiliary memory comprises a static random access memory ("SRAM") device.

40. (Previously Presented) The processor-based system of claim 38 wherein the control circuit comprises:

a refresh controller coupled to the at least one DRAM array, the refresh controller being operable to refresh the at least one DRAM array one block at a time; and

a control buffer structured to receive a memory command and to generate the first, second and third control signals corresponding thereto.

41. (Previously Presented) The processor-based system of claim 38 wherein the plurality of blocks of the at least one DRAM array are physically part of a single DRAM array.

42. (Previously Presented) The processor-based system of claim 38 wherein the input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the at least one DRAM array while a second pair of input/output lines may be coupled to another block of the at least one DRAM array.

43. (Previously Presented) The processor-based system of claim 38, further comprising a second auxiliary memory operable to store data in the event the first auxiliary memory is busy storing data or reading or writing data.

44. (Previously Presented) A processor-based system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a system controller coupled to the processor bus;

an integrated circuit system memory and cache system coupled to the processor through the system controller, comprising:

at least one DRAM array divided into a plurality of blocks;

an auxiliary memory coupled to the at least one DRAM array for direct transfer of data from the auxiliary memory to any block of the at least one DRAM array if the block of the at least one DRAM array is not being refreshed; and

an input/output circuit coupled to the at least one DRAM array and the auxiliary memory, the input/output circuit being operable to store write data in a block of the at least one DRAM array to which the write data was directed, and to store write data directed to any block of the at least one DRAM array in the auxiliary memory if the block to which the write data was directed is being refreshed.

45. (Currently Amended) The processor-based system of claim 44 wherein the plurality of blocks of the at least one DRAM array ~~is~~are physically part of a single DRAM array.

46. (Currently Amended) The processor-based system of claim 44 wherein the ~~an~~ input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the at least one DRAM array while a second pair of input/output lines may be coupled to another block of the at least one DRAM array.

47. (Previously Presented) The processor-based system of claim 44 wherein the auxiliary memory comprises a static random access memory device.

48. (Previously Presented) A method of caching data stored in an integrated circuit dynamic random access memory ("DRAM") device having a plurality of blocks each of which may be refreshed, the method comprising:

providing an auxiliary memory in the integrated circuit DRAM;

addressing a first block of the DRAM in an attempt to write data into the first block of the DRAM;

if the first block of the DRAM is being refreshed during the attempt, writing the data into the auxiliary memory;

after the first block of the DRAM is no longer being refreshed, transferring data stored in the auxiliary memory to the first block of the DRAM.

49. (Previously Presented) The method of claim 48 wherein the DRAM further includes an alternate auxiliary memory and wherein in the method further comprises:

writing the data into the alternate auxiliary memory if the auxiliary memory is storing data or data are being written to or read from the auxiliary memory when the first block of DRAM is being refreshed during the attempt to write data into the first block of the DRAM; and

after the first block of the DRAM is no longer being refreshed, transferring data stored in the alternate auxiliary memory to the first block of the DRAM.

50. (Previously Presented) The method of claim 48 wherein the auxiliary memory comprises static random access memory.

51. (Currently Amended) The method of claim 48 further comprising writing data into ~~the~~a first SRAM if ~~the~~a second block of the DRAM is being refreshed during the attempt to write the data into the second block and data is not being transferred from the auxiliary memory to the first block of the DRAM.

52. (Previously Presented) The method of claim 48 further comprising writing the data into the first block of the DRAM if the first block of the DRAM is not being refreshed during the attempt.

53. (Currently Amended) The method of claim 48 further comprising:

addressing ~~a~~the first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the DRAM.

54. (Previously Presented) The method of claim 53 wherein the act of outputting data from the first block of the DRAM is accomplished regardless of whether or not the first block of memory is being refreshed.

55. (Previously Presented) The method of claim 48 further comprising:

addressing the first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the DRAM; and

caching the data output from the first block of the DRAM in the auxiliary memory.

56. (Previously Presented) The method of claim 55 further comprising

addressing the first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the auxiliary memory.

57. (Currently Amended) A method of caching data stored in an integrated circuit dynamic random access memory ("DRAM") device having a plurality of blocks each of which may be refreshed, the method comprising:

providing a DRAM having a plurality of blocks each of which may be refreshed, each of the blocks including DRAM memory cells arranged in rows and columns;

providing a first auxiliary memory and a second auxiliary memory each of which has sufficient capacity to store a row of data from a block of the DRAM;

sequentially attempting to write data to blocks of the DRAM;

if a block to which data is ~~attempting~~attempted to be written is being refreshed, writing the data to the first auxiliary memory;

when the refresh of a block has been completed, transferring data from the first auxiliary memory to which the data had been written to a block of the DRAM to which data was attempted to be written; and

if a block to which data is ~~attempting~~attempted to be written is being refreshed and data is being transferred from the first auxiliary memory to a block of the DRAM, writing the data to the second auxiliary memory.

58. (Previously Presented) The method of claim 57 wherein each of the first and second auxiliary memories comprises a static random access memory.

59. (Currently Amended) The method of claim 57 further comprising, if the block to which data is ~~attempting~~attempted to be written is not being refreshed, writing the data to the block of the DRAM.

60. (Previously Presented) The method of claim 57 further comprising:

attempting to read data from a block of the DRAM; and

outputting data from the block of the DRAM to which an attempt to read data is directed.

61. (Previously Presented) The method of claim 60 wherein the act of outputting data from the block of the DRAM is accomplished regardless of whether or not the block of memory is being refreshed.

62. (Previously Presented) The method of claim 60 further comprising:

attempting to read data from a block of the DRAM;

outputting data from the block of the DRAM to which an attempt to read data is directed and

caching the data output from the block of the DRAM in one of the first and second auxiliary memories.